IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Confirmation No.: 2396
ALLOTT *et. al.*	Art Unit: 2687
Application No.: 09/813,420	Examiner: Bhattacharya, Sam
Filed: October 31, 2002	Atty. Docket: 1875.8080000
For: **DC Offset Correction for Use in a Direct-Conversion Radio Architecture**	

Brief on Appeal to the Board of Patent Appeals and Interferences Under 37 C.F.R § 41.37

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Commissioner for Patents
PO Box 1450
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Sir:

A Notice of Appeal from the final rejection of claims 2-10 for the above-captioned U.S. Patent Application was filed on July 25, 2005 appealing the decision of the Examiner in the Final Office Action mailed January 25, 2005, maintaining the rejection of claims 2-10.

In support of the Notice of Appeal, Appellants hereby file an appeal brief as required under 37 C.F.R. § 41.37(a). Appellants have also filed herewith the fee for filing a brief in support of an appeal as set forth in 37 C.F.R. § 41.37(a)(2)

The Commissioner is hereby authorized to charge any fee deficiency, or credit any overpayment, to Deposit Account No. 19-0036.

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I. *Real Party in Interest (37 C.F.R. § 41.37(c)(1)(i))*

The real party of interest is Broadcom Corporation, having its principal place of business at 16215 Alton Parkway, Irvine, California, 92618-3636. An assignment assigning all right, title, and interest in and to the patent application from the inventors to Broadcom was recorded in the U.S. Patent & Trademark Office on July 17, 2001 at Reel 012012, Frame 0653.

II. Related Appeals and Interferences (37 C.F.R. § 41.37(c)(1)(ii))

To the best of knowledge of Appellants, Appellants' legal representative, and Appellants' assignee, there are no other appeals or interferences which will directly affect or be directly affected or have a bearing on a decision by the Board of Patent Appeals and Interferences ("the Board") in the pending appeal.

III. Status of the Claims (37 C.F.R. § 41.37(c)(1)(iii))

This application was originally filed as U.S. Application No. 09/813,420 on March 20, 2001 with 10 claims. In an Office Action mailed February 26, 2004, claims 1-10 were rejected. In the Amendment and Reply filed on August 26, 2004, Appellants cancelled claim 1 without prejudice and amended claims 2 and 7.

The pending claims 2-10 were finally rejected in an Office Action mailed January 25, 2005. No claim stands allowed.

Accordingly, the claims on appeal are claims 2-10. A copy of the claims on appeal can be found in the attached Claims Appendix as required under 37 C.F.R. § 41.37(c)(1)(viii).

IV. Status of Amendments (37 C.F.R. § 41.37(c)(1)(iv))

All amendments have been entered. The Final Office Action dated January 25, 2005 responded to and acknowledged Appellants' amendment filed August 26, 2004.

V. Summary of Claimed Subject Matter (37 C.F.R. § 41.37(c)(1)(v))

A problem characteristic of direct-conversion receivers relates to the down-converted band being centered around zero frequency. Centering of the down-converted band around zero frequency can be problematic, since any extraneous DC offsets may be unwantedly amplified in the I and Q channels of the receiver. The amplified DC offsets can corrupt the received signal and can even impede reception if the DC offsets are amplified to levels that saturate subsequent stages of the receiver.

The present invention relates to a direct-conversion type receiver capable of removing DC offsets.

Independent claim 1 is directed to a radio receiver 20 (FIG. 2) comprising an amplifier 216 configured to receive and amplify an intermediate frequency modulated signal having in-phase and quadrature phase DC components (Specification, page 6, lines 7-8); an analog-to-digital converter 218 configured to receive the amplified intermediate frequency modulated signal and convert it to a digital signal (Specification, page 6, lines 8-9); a demodulator 220 operable to demodulate the digital signal (Specification, page 6, line 9); DC offset calibration means 224 coupled to the demodulator operable to provide in-phase and quadrature DC offset correction signals (I_DAC_OFFSET_WORD and Q_DAC_OFFSET_WORD) to compensate

for the in-phase and quadrature phase DC components at the input of the amplifier (Specification, page 9, lines 1-3); and delay measurement means 223 coupled to the demodulator 220 operable to determine a delay vector characterizing the in-phase and quadrature phase DC components (Specification, page 7, lines 3-5).

Independent claim 5 is also directed to a radio receiver 20 comprising a receiving stage (Specification, page 5, line 23) configured to receive a radio signal (RF input signal in FIG. 2); a first mixer stage (mixers 200 and 202) operable to downconvert the radio frequency signal to a first intermediate frequency in-phase signal and a first intermediate frequency quadrature phase signal (Specification, page 5, lines 24-27); first and second low pass filters (204 and 206) configured to receive and low pass filter the first intermediate frequency in-phase and quadrature phase signals (Specification, page 5, lines 28-30); a second mixer stage (mixers 208 and 210) operable to upconvert the filtered first intermediate frequency in-phase and quadrature phase signals and provide a second intermediate frequency in-phase signal and a second intermediate frequency quadrature phase signal (Specification, page 5, line 30 - page 6, line 2); a summer 212 operable to subtract the second intermediate frequency quadrature phase signal from the second intermediate frequency in-phase signal to provide an integrated signal (Specification, page 6, lines 3-5); an automatic gain control stage 216 coupled to the summer 212 and operable to amplify the integrated signal (Specification, page 6, lines 7-8); an analog-to-digital converter 218 operable to convert the amplified integrated signal to a digital signal (Specification, page 6, lines 8-9); a demodulator 220 operable to demodulate the digital signal (Specification, page 6, line 9); and delay measurement means 223 for determining a

delay vector from inputs of the low pass filters (204 and 206) to an output of the demodulator 220 (Specification, page 7, lines 3-5).

An feature of the claimed invention is the ability to separate intermingled in-phase and quadrature phase DC offsets using a determined signal delay, and then use the separated DC offsets to correct for DC offsets at the input of the receiver. Independent claim 7 recited steps for determining the signal delay. Independent claims 8 and 10 recite steps of methods of compensating for DC offsets at the input of the receiver. Independent claim 9 recites steps for setting signal levels of in-phase and quadrature phase components of a radio receiver between a minimum and a maximum threshold voltage. This method recited in claim 9 may be used by the methods of claims 8 and 10.

Independent claim 7 is directed to a method of determining a signal delay between inputs of a first and second low pass filters (204 and 206) of a dual mixer stage radio receiver 20 and an output of the receiver's demodulator 220. The method of claim 7 comprises the steps of: applying a first known voltage (-VDCI) to an input of an in-phase mixer 208 of the second mixer stage (Specification, page 7, line 29); applying a second known voltage (VDCQ = 0) to an input of a quadrature phase mixer 210 of the second mixer stage (Specification, page 7, line 30); setting the gain of an automatic gain control stage 216, coupled to the second mixer stage, to a full gain (Specification, page 7, line 12); measuring first in-phase and first quadrature phase components at the output of the demodulator 220 (Specification, page 7, lines 32-33); decreasing the gain of the automatic gain control stage 216 by a predetermined amount if the value of either first component is greater than a

predetermined maximum threshold value (Specification, page 8, lines 1-4); storing the first in-phase and quadrature phase components ($VN3_I(1)$ and $VN3_Q(1)$) if the value of each component is less than the predetermined maximum threshold value (Specification, page 8, lines 4-7); applying the negative of the first known voltage (VDCI) to the input of the in-phase mixer 208 (Specification, page 8, line 8); applying the second known voltage (VDCQ = 0) to the input of the quadrature phase mixer 210 (Specification, page 8, line 9); measuring second in-phase and second quadrature phase components at the output of the demodulator 220 (Specification, page 8, lines 11-12); decreasing the gain of the automatic gain control stage 216 by a predetermined amount if the value of either second component is greater than the predetermined maximum threshold value; storing the second in-phase and quadrature phase components ($VN3_I(2)$ and $VN3_Q(2)$) if the value of each second component is less than the predetermined maximum threshold value (Specification, page 8, lines 12-13); and using the first and second quadrature phase components to compute the signal delay (Specification, page 8, lines 14-15).

Independent claim 8 is directed to a method of compensating for DC offset voltages present at an input of a low noise amplifier of a dual mixer stage radio receiver 20. The method of claim 8 comprises the steps of: determining a signal delay between an output of a second mixer stage of the dual mixer stage radio receiver, said signal delay characterizing in-phase and quadrature phase components of the DC offset voltage present at the input of the low noise amplifier (Specification, page 8, lines 20-23); using the predetermined signal delay to separate and define digital representations (I_DAC_OFFSET_WORD and Q_DAC_OFFSET_WORD) of the in-

phase DC offset voltage component and the quadrature phase DC offset voltage component (Specification, page 8 line 22 - page 9 line 3); making the digital representation of each of the in-phase and quadrature phase components more positive or more negative if it is more negative or more positive than a predetermined minimum threshold or maximum threshold (Specification, page 9 line 28 - page 10 line 2); and performing the above sequence of steps a predetermined number of times to reduce the DC offset voltage at the input of the low noise amplifier (Specification, page 10, lines 10-12).

Independent claim 9 is directed to a method of setting signal levels of in-phase and quadrature phase components of a radio receiver 20 between a minimum threshold voltage and a maximum threshold voltage, the method comprising the steps of: (a) setting the gain of an automatic gain control 216 to a gain value at which the signal levels of the in-phase and quadrature phase components are less than or equal to the maximum threshold voltage (Specification, page 7, lines 22-24); (b) comparing the signal levels of the in-phase and quadrature phase components to a predetermined minimum threshold value (Specification, page 10, lines 4-5); (c) increasing the gain of the automatic gain control stage 216 by a predetermined amount; and (d) repeating steps (b) and (c) until the signal levels of the in-phase and quadrature phase components are greater than or equal to the predetermined minimum threshold value (Specification, page 10, lines 6-7).

Independent claim 10 is directed to a method of compensating for DC offset voltages at inputs of in-phase and quadrature phase low pass filters (204 and 206) of a dual mixer stage radio receiver 20. The method of claim 10 comprises the steps of:

determining a signal delay vector between the inputs of the low pass filters, said signal delay vector characterizing in-phase and quadrature phase components of DC offset voltages at the inputs of the low pass filters (Specification, page 8, lines 20-23); using the signal delay vector to separate and define in-phase and quadrature phase multiplication factors associated with the in-phase and quadrature phase DC offsets (Specification, page 8, lines 22-27); incrementally adjusting the signal level of the in-phase component to a more positive or more negative value if the in-phase multiplication factor has a negative or positive value, respectively; and incrementally adjusting the signal value of the quadrature phase component to a more positive or more negative value if the quadrature phase multiplication factor has a negative or positive value, respectively (Specification, page 9, line 25 - page 10, line 2).

VI. Grounds of Rejection to be Reviewed on Appeal (37 C.F.R. § 41.37(c)(1)(vi))

In the final Office Action mailed January 25, 2005, the Examiner rejected claims 2-4 as allegedly being anticipated by Luz *et al.*, U.S. Patent No. 6,321,073 (hereinafter Luz), claim 9 as allegedly being anticipated by Zarubinsky *et al.*, U.S. Patent Application Publication No. 2002/0114413 (hereinafter Zarubinsky), claims 5-6 as allegedly being unpatentable over Luz in view of Galal *et al.*, U.S. Patent No. 6,161,004 (hereinafter Galal), and claims 7, 8, and 10 as being allegedly unpatentable over Zarubinsky in view of Galal.

Accordingly, the grounds of rejection to be reviewed on appeal are:

A. Rejection of claims 2-4 under 35 U.S.C. §102 over U.S. Patent No. 6,321,073 to Luz.

B. Rejection of claim 9 under 35 U.S.C. §102 over U.S. Patent Application Publication No. 2002/0114413 to Zarubinsky.

C. Rejection of claims 5-6 under 35 U.S.C. §103 over Luz in view of U.S. Patent No. 6,161,004 to Galal.

D. Rejection of claims 7, 8, and 10 under 35 U.S.C. §103 over Zarubinsky in view of Galal.

VII. Argument (37 C.F.R. § 41.37(c)(1)(vii))

A. ***Ground A.*** Rejection of claims 2-4 under 35 U.S.C. §102 over U.S. Patent No. 6,321,073 to Luz.

1. The Final Rejection

A Final Office Action was mailed on January 25, 2005, rejecting claims 2-4 under U.S.C. § 102(e) as being anticipated by Luz.

2. Luz does not anticipate claims 2-4

Independent claim 2 recites, among other features, a "delay measurement means coupled to the demodulator operable to determine a delay vector characterizing the in-phase and quadrature phase DC components". This feature of claim 2 is described in detail in the specification (page 7, line 8 - page 9, line 27).

In the final rejection of claim 2, the Examiner refers to Luz (col. 4, lines 20-38), as allegedly teaching this feature. Luz (col. 4, lines 28-38) describes the operation of a feedforward DC compensation circuit (in-phase DC compensation circuit 334 or quadrature phase DC compensation circuit 336). The feedforward DC compensation circuit of Luz performs an averaging function of input digital samples (col. 4, lines 26-30), a squaring function of the computed average (col. 4, lines 31-35), and a truncation function to result in a DC offset error signal (in-phase DC offset error 360a or quadrature phase DC offset error 360b). Accordingly, none of the functions performed by feedforward compensation circuits 360a and 360b of Luz corresponds to a delay measurement function that determines a delay vector, as recited in independent claim 2.

In response to Appellants' arguments (in their Reply filed August 26, 2004), the Examiner disagrees with Appellants' argument that Luz provides no delay measurement means, and further re-asserts that each of DC offset compensation circuits 334 and 336 "*determines a delay vector, corresponding to the DC offset compensation*" in the in-phase and quadrature phase paths, respectively. Appellants found no indication or suggestion anywhere in Luz to support this claim by the Examiner. The Examiner further argues that claim 2 does not recite "a delay vector angle", a term which appeared in Appellants' argument (in their Reply filed August 26, 2004). Appellants would like to point out that the term "delay vector angle" was only used to further clarify this feature of claim 2. In fact, it is well known in the art that a "delay vector" and a "delay vector angle" are related in a straightforward

manner, and that the determination of a "delay vector angle" easily follows from the determination of a "delay vector".

Independent claim 2 further recites, among other features, "DC offset calibration means coupled to the demodulator operable to provide in-phase and quadrature phase DC offset correction signals to compensate for the in-phase and quadrature phase DC components at the input of the amplifier". This feature of claim 2 is described in detail in the specification (page 9, line 1 - page 10, line 15). According to this feature, the DC offset correction signals are provided by the DC offset calibration means 224 to be separately applied to mixers 208 and 210, respectively. The application of the DC offset correction signals to mixers 208 and 210 reduces I and Q DC offset components in subsequently measured samples at the output of demodulator 220.

In the final rejection of claim 2, the Examiner refers to feedforward DC offset compensation circuit 202 of Luz and cites from Luz (col. 3, lines 10-14) that "*the feedforward DC offset compensation circuit 202 generates an in-phase digital error signal 360a (see FIG. 3A) and a quadrature phase DC error signal 360b to remove DC offsets introduced by the ADC or other sources. These signals are combined and subtracted from the signal*". (Office Action, page 2 (emphasis added)). The Examiner accordingly claims that feedforward DC offset compensation circuit 202 corresponds to the DC offset calibration means recited in claim 2.

Appellants point out that the DC offset calibration means recited in claim 2 and the feedforward DC offset compensation circuit 202 of Luz have different functions. This is obvious based on the fact that the DC offset compensation architecture according to the present invention is a feedback architecture (DC offset correction

signals are fed back at the input stage of the receiver to reduce subsequent DC offsets) while Luz teaches a feedforward system (DC offsets are calculated and subtracted at the same stage of the receiver). The different functions of the two circuits can be further determined by examining the nature of the inputs and outputs of each circuit. For example, DC offset calibration means 224 recited in claim 2 receives a delay vector and outputs digital correction signals (I_DAC_OFFSET_WORD and Q_DAC_OFFSET_WORD), which are applied separately (see FIG. 2) to mixers 226 and 222 to reduce DC offset components. In contrast, DC offset compensation circuit 202 of Luz receives a gain compensated signal 112 and outputs in-phase and quadrature phase error signals 360a and 360b, which are combined and subtracted from the signal 112 (col. 3, lines 10-14). DC offset compensation circuit 202 therefore does not correspond to the DC offset calibration means recited in claim 2.

For at least the reasons provided above, Luz does not teach or suggest each and every feature of independent claim 2. Claim 2 is therefore patentable over Luz, and the rejection of claim 2 must be reversed.

Claims 3 and 4 depend from claim 2. For at least these reasons provided above with respect to claim 2, and further in view of their own features, claims 3 and 4 are patentable over Luz. The rejection of claims 3 and 4 must be reversed.

Ground B. Rejection of claim 9 under 35 U.S.C. §102 over U.S. Patent Application Publication No. 2002/0114413 to Zarubinsky.

1. The Final Rejection

A Final Office Action was mailed on January 25, 2005, rejecting claim 9 under U.S.C. § 102(e) as being anticipated by Zarubinsky.

2. Zarubinsky does not anticipate claim 9

Independent claim 9 recites, among other features, "setting the gain of an automatic gain control to a gain value at which the signal levels of the in-phase and quadrature phase components are less than or equal to the maximum threshold voltage" and "comparing the signal levels of the in-phase and quadrature phase components to a predetermined minimum threshold value".

In the final rejection of claim 9, the Examiner refers to Zarubinsky (page 2, col. 1, paragraphs [0028], [0030], and [0031]; and page 5, col. 2, paragraphs [0089] to 0092]) as allegedly teaching the above recited features of claim 9.

The above noted paragraphs of Zarubinsky describe the need for having equally matched in-phase and quadrature phase channel gains and seem to suggest a technique for maintaining the channel gains equalized. However, none of the subject matter described in these paragraphs or anywhere in Zarubinsky teach or suggest the above recited features of independent claim 9.

Further, in response to Appellants' arguments (in their Reply filed August 26, 2004), the Examiner claims that by matching the gains of the I and Q paths, Zarubinsky sets the gain to a maximum threshold voltage. Appellants found no indication or suggestion in Zarubinsky to support this claim by the Examiner.

For at least the reasons provided above, Zarubinsky does not teach or suggest each and every feature of independent claim 9. Claim 9 is therefore patentable over Zarubinsky, and the rejection of claim 9 must be reversed.

C. ***Ground C.*** Rejection of claims 5-6 under 35 U.S.C. §103 over Luz in view of U.S. Patent No. 6,161,004 to Galal.

1. The Final Rejection

A Final Office Action was mailed on January 25, 2005, rejecting claims 5-6 under U.S.C. § 103(a) as being unpatentable over Luz in view of Galal.

2. Claims 5-6 are patentable over Luz in view Galal

Independent claim 5 recites, among other features, a "delay measurement means for determining a delay vector from inputs of the low pass filters to an output of the demodulator". This feature of claim 5 is described in detail in the specification (page 7, line 8 - page 9, line 27).

In the final rejection of claim 5, the Examiner refers to Luz (col. 4, lines 20-38) as allegedly teaching this feature.

Appellants note that this feature of claim 5 is similar to the "delay measurement means" feature of independent claim 2, distinguished above with respect to Luz. Accordingly, for at least the same reasons provided above with respect to independent claim 2, Luz does not teach or suggest a "delay measurement means for determining a delay vector" as recited in claim 5. Further, Galal does not overcome the deficiencies of Luz with respect to claim 5, as described above. Accordingly, independent claim 5 is patentable over Luz and Galal. The rejection of claim 5 must be reversed.

Claim 6 depends from independent claim 5. For at least these reasons provided above with respect to claim 5, claim 6 is patentable over Luz and Galal. Further, claim 6 is patentable over Luz and Galal in view of its own "DC offset calibrator"

feature, which is similar to the "DC offset calibration means" feature of claim 2. The "DC offset calibration means" feature of claim 2 has been distinguished above with respect to Luz, and is not taught or suggested in Galal.

Claim 6 is therefore patentable over Luz and Galal. The rejection of claim 6 must be reversed.

D. ***Ground D.*** Rejection of claims 7, 8, and 10 under 35 U.S.C. §103 over Zarubinsky in view of Galal.

1. The Final Rejection

A Final Office Action was mailed on January 25, 2005, rejecting claims 7, 8, and 10 under U.S.C. § 103(a) over Zarubinsky in view of Galal.

2. Claim 7 is patentable over Zarubinsky in view of Galal

Independent claim 7 is directed to a method for determining a signal delay between inputs of first and second low pass filters of a dual mixer stage radio receiver and an output of the receiver's demodulator. The method of claim 7 recites specific steps for measuring in-phase and quadrature phase components at the output of the receiver's demodulator after applying specific voltage values at inputs of a second mixer stage of the receiver, and using the measured components to compute a signal delay. Support for the method of claim 7 can be found in detail in the specification (page 7, line 8 - page 8, line 27).

Independent claim 7 recites, among other features, "using the first and second quadrature phase components to compute the signal delay". Independent claim 7 further recites, among other features, the steps of "applying a first known voltage to

an input of an in-phase mixer of the second mixer stage", "applying a second known voltage to an input of a quadrature phase mixer of the second mixer stage", "setting the gain of an automatic gain control stage, coupled to the second mixer, to a full gain", and "measuring first in-phase and first quadrature phase components at the output of the demodulator".

In the final rejection of claim 7, the Examiner refers to Zarubinksy (page 3, col. 1, paragraph [0044] - page 5, col. 1, paragraph [0082]; and Figures 5-8) as allegedly teaching the above recited features of claim 7. However, the above noted paragraphs of Zarubinsky are directed to the operation of a gain controller and do not teach or suggest any of the above recited features of claim 7. Appellants further found no indication or suggestion anywhere in Zarubinsky teaching the above recited features.

Further, in response to Appellants' arguments (in their Reply filed August 26, 2004), the Examiner claims that delay stages 234 and 244 in Zarubinsky "*clearly teach using first and second quadrature phase components to compute the signal delay*". However, as described in Zarubinsky (page 3, col. 1, paragraph [0047), delay stages 234 and 244 are used for synchronization purposes. In addition, as described in Zarubinsky (page 5, col. 1, paragraphs [0073]-[0077]) with respect to delay stage 207, delay stage 207 appears to act on a signal X'_D, which is a function of a comparator 221 output and does not correspond to in-phase or quadrature phase components (which are denoted by I_D and Q_D in Zarubinsky). Accordingly, Zarubinsky does not teach or suggest "using the first and second quadrature phase components to compute the

signal delay". This is in addition to Zarubinsky not teaching or suggesting any of the other above recited features of independent claim 7.

Accordingly, Zarubinsky does not teach or suggest at least the above recited features of claim 7. Galal also fails to teach or suggest at least these features of claim 7. Claim 7 is therefore patentable over Zarubinsky in view of Galal. The rejection of claim 7 must be reversed.

3. Claim 8 is patentable over Zarubinsky in view of Galal

Independent claim 8 is directed to a method of compensating for DC offset voltages present at an input of a low noise amplifier of a dual mixer stage radio receiver.

Independent claim 8 recites, among other features, "determining a signal delay between an output of a second mixer stage of the dual mixer stage radio receiver, said signal delay characterizing in-phase and quadrature phase components of the DC offset voltage present at the input of the low noise amplifier" and "using the determined signal delay to separate and define digital representations of the in-phase DC offset voltage and the quadrature phase DC offset voltage component". Support for these features of claim 8 can be found in the Specification (page 8, line 20 - page 9, line 3).

In the final rejection of claim 8, the Examiner refers to Zarubinksy (page 5, col. 1, paragraph [0077]; and page 5, col. 2, paragraphs [0094]-[0095]) as allegedly teaching the above recited features of claim 8. However, as discussed above with respect to claim 7, Zarubinsky (page 5, col. 1, paragraph [0077]) does not teach or suggest "determining a signal delay" that characterizes in-phase and quadrature phase

components of a DC offset as recited in claim 8. Further, Zarubinsky (page 5, col. 2, paragraphs [0094]-[0095]) is directed to the operation of an offset compensation loop and does not teach or suggest "using the determined signal delay to separate and define digital representation of the in-phase DC offset voltage and the quadrature phase DC offset voltage component" as recited in claim 8.

Accordingly, Zarubinsky does not teach or suggest at least the above recited features of independent claim 8. Galal also fails to teach or suggest at least these features of claim 8. Claim 8 is therefore patentable over Zarubinsky in view of Galal. The rejection of claim 8 must be reversed.

4. Claim 10 is patentable over Zarubinsky in view of Galal

Independent claim 10 is directed to a method of compensating for DC offset voltages at inputs of in-phase and quadrature phase low pass filters of a dual mixer stage radio receiver.

Independent claim 10 recites, among other features, "determining a signal delay vector between the inputs of the low pass filters, said signal delay vector characterizing in-phase and quadrature phase components of the DC offset voltages at the inputs of the low pass filters" and "using the signal delay vector to separate and define digital in-phase and quadrature phase multiplication factors associated with the in-phase and quadrature phase DC offsets". Support for these features of claim 10 can be found in the Specification (page 8, line 20 - page 9, line 3).

In the final rejection of claim 10, the Examiner refers to Zarubinksy (page 5, col. 1, paragraph [0077]; and page 5, col. 2, paragraphs [0094]-[0095]) as allegedly teaching the above recited features of claim 10. However, as discussed above with

respect to claim 7, Zarubinsky (page 5, col. 1, paragraph [0077]) does not teach or suggest "determining a signal delay vector" that characterizes in-phase and quadrature phase components of DC offset voltages as recited in claim 10. Further, Zarubinsky (page 5, col. 2, paragraphs [0094]-[0095]) is directed to the operation of an offset compensation loop and does not teach or suggest "using the signal delay vector to separate and define digital in-phase and quadrature phase multiplication factors associated with the in-phase and quadrature phase DC offsets " as recited in claim 10.

Accordingly, Zarubinsky does not teach or suggest at least the above recited features of independent claim 10. Galal also fails to teach or suggest at least these features of claim 10. Claim 10 is therefore patentable over Zarubinsky in view of Galal. The rejection of claim 10 must be reversed.

VIII. Conclusion

The subject matter of claims 2-10 are patentable over the cited prior art. Therefore, Appellants respectfully request that the Board reverse the Examiner's final rejection of these claims under 35 U.S.C. §102 and 35 U.S.C. §103 and remand this application for issue.

Respectfully submitted,
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CLAIMS APPENDIX

1. (*cancelled*)

2. (*amended*) A radio receiver, comprising:

an amplifier configured to receive and amplify an intermediate frequency modulated signal having in-phase and quadrature phase DC components;

an analog-to-digital converter configured to receive the amplified intermediate frequency modulated signal and convert it to a digital signal;

a demodulator operable to demodulate the digital signal;

DC offset calibration means coupled to the demodulator operable to provide in-phase and quadrature phase DC offset correction signals to compensate for the in-phase and quadrature phase DC components at the input of the amplifier; and

delay measurement means coupled to the demodulator operable to determine a delay vector characterizing the in-phase and quadrature phase DC components.

3. (*original*) The radio receiver of claim 2, wherein the delay vector is used by the DC offset calibration means to provide a digital representation of the in-phase and quadrature phase DC offset correction signals.

4. (*original*) The radio receiver of claim 3, further comprising:

a first digital-to-analog converter configured to receive a in-phase component of the digital representation of the in-phase DC offset correction signal for mixing with an in-phase signal and an intermediate frequency carrier signal;

a second digital-to-analog converter configured to receive a quadrature phase component of the digital representation of the quadrature phase DC offset correction signal for mixing with a quadrature signal and the intermediate frequency carrier signal; and

a summer operable to subtract the mixed quadrature phase signal and quadrature phase DC offset correction signal component from the mixed in-phase signal and in-phase DC offset correction signal to provide a DC compensated intermediate frequency modulated signal at the input of the low noise amplifier.

5. (*original*) A radio receiver, comprising:

a receiving stage configured to receive a radio signal;

a first mixer stage operable to downconvert the radio frequency signal to a first intermediate frequency in-phase signal and a first intermediate quadrature phase signal;

first and second low pass filters configured to receive and low pass filter the first intermediate frequency in-phase and quadrature phase signals;

a second mixer stage operable to upconvert the filtered first intermediate frequency in-phase and quadrature phase signals and provide a second intermediate frequency in-phase signal and a second intermediate frequency quadrature phase signal;

a summer operable to subtract the second intermediate frequency quadrature phase signal from the second intermediate frequency in-phase signal to provide an integrated signal;

an automatic gain control stage coupled to the summer and operable to amplify the integrated signal;

an analog-to-digital converter operable to convert the amplified integrated signal to a digital signal;

a demodulator operable to demodulate the digital signal; and

delay measurement means for determining a delay vector from inputs of the low pass filters to an output of the demodulator.

6. (*original*) The radio receiver of claim 5, further comprising:

a DC offset calibrator coupled to the delay measurement means;

an in-phase digital-to-analog converter coupled between the DC offset calibrator and the second mixer stage; and

a quadrature phase digital-to-analog converter coupled between the DC offset calibrator and the second mixer stage,

wherein the in-phase digital-to-analog converter is operable to provide an in-phase DC offset compensation signal for the automatic gain control stage and the quadrature phase digital-to-analog converter is operable to provide a quadrature phase DC offset compensation signal for the automatic gain control stage.

7. (*amended*) A method of determining a signal delay between inputs of first and second low pass filters of a dual mixer stage radio receiver and an output of the receiver's demodulator, the method comprising the steps of:

applying a first known voltage to an input of an in-phase mixer of the second mixer stage;

applying a second known voltage to an input of a quadrature phase mixer of the second mixer stage;

setting the gain of an automatic gain control stage, coupled to the second mixer stage, to a full gain; measuring first in-phase and first quadrature phase components at the output of the demodulator;

decreasing the gain of the automatic gain control stage by a predetermined amount if the value of either first component is greater than a predetermined maximum threshold value;

storing the first in-phase and quadrature phase components if the value of each component is less than the predetermined maximum threshold value;

applying the negative of the first known voltage to the input of the in-phase mixer;

applying the second known voltage to the input of the quadrature phase mixer;

measuring second in-phase and second quadrature phase components at the output of the demodulator;

decreasing the gain of the automatic gain control stage by a predetermined amount if the value of either second component is greater than the predetermined maximum threshold value;

storing the second in-phase and quadrature phase components if the value of each second component is less than the predetermined maximum threshold value; and

using the first and second quadrature phase components to compute the signal delay.

8. (*original*) A method of compensating for DC offset voltages present at an input of a low noise amplifier of a dual mixer stage radio receiver, the method comprising the steps of:

determining a signal delay between an output of a second mixer stage of the dual mixer stage radio receiver, said signal delay characterizing in-phase and quadrature phase components of the DC offset voltage present at the input of the low noise amplifier;

using the determined signal delay to separate and define digital representations of the in-phase DC offset voltage component and the quadrature phase DC offset voltage component;

making the digital representation of each of the in-phase and quadrature phase components more positive or more negative if it is more negative or more positive than a predetermined minimum threshold or maximum threshold; and

performing the above sequence of steps a predetermined number of times to reduce the DC offset voltage at the input of the low noise amplifier.

9. (*original*) A method of setting signal levels of in-phase and quadrature phase components of a radio receiver between a minimum threshold voltage and a maximum threshold voltage, the method comprising the steps of:

(a) setting the gain of an automatic gain control to a gain value at which the signal levels of the in-phase and quadrature phase components are less than or equal to the maximum threshold voltage;

(b) comparing the signal levels of the in-phase and quadrature phase components to a predetermined minimum threshold value;

(c) increasing the gain of the automatic gain control stage by a predetermined amount; and

(d) repeating steps (b) and (c) until the signal levels of the in-phase and quadrature phase components are greater than or equal to the predetermined minimum threshold value.

10. (*original*) A method of compensating for DC offset voltages at inputs of in-phase and quadrature phase low pass filters of a dual mixer stage radio receiver, said method comprising the steps of:

determining a signal delay vector between the inputs of the low pass filters, said signal delay vector characterizing in-phase and quadrature phase components of DC offset voltages at the inputs of the low pass filters;

using the signal delay vector to separate and define in-phase and quadrature phase multiplication factors associated with the in-phase and quadrature phase DC offsets;

incrementally adjusting the signal level of the in-phase component to a more positive or more negative value if the in-phase multiplication factor has a negative or positive value, respectively; and

incrementally adjusting the signal value of the quadrature phase component to a more positive or more negative value if the quadrature phase multiplication factor has a negative or positive value, respectively.

EVIDENCE APPENDIX

Not applicable.

RELATED PROCEEDINGS APPENDIX

Not applicable.